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VDE ETG

Fraunhofer IISB
Fraunhofer Institute for Integrated Systems and Device Technology IISB

Milliseconds Power Cycling (PC_{msec}) driving bipolar degradation in Silicon Carbide Power Devices

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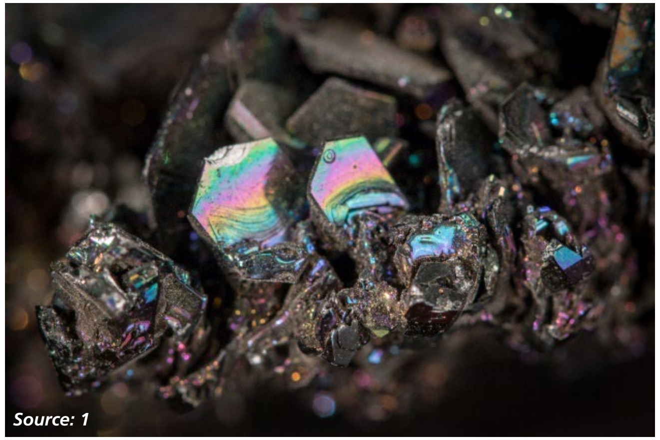
In collaboration with
nexperia
TUHH Technische Universität Hamburg

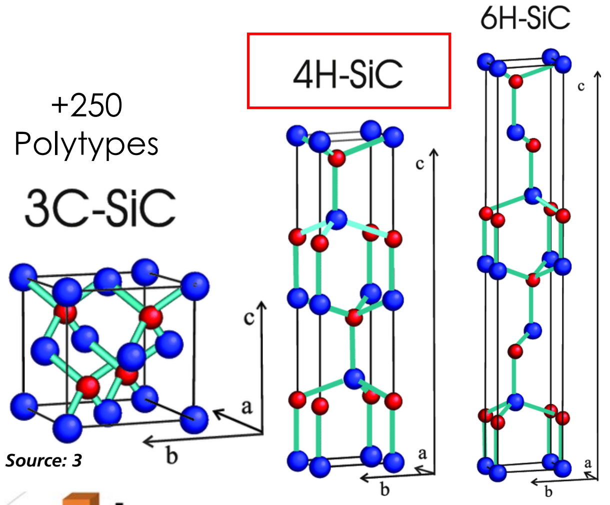
Silicon Carbide (SiC)?

From meteorites to power electronics


Source: 1


Source: 2

+250 Polytypes



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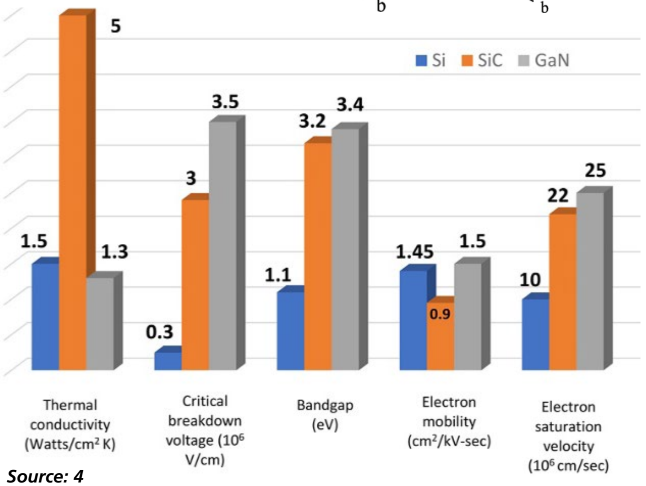

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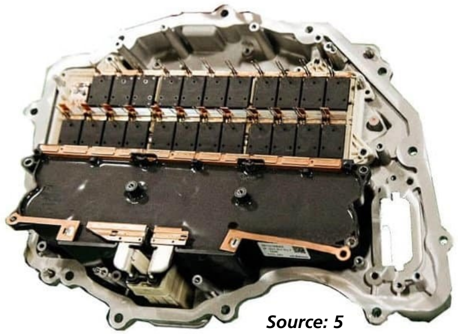
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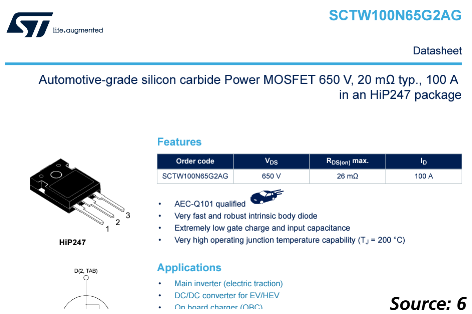
life.augmented

SCTW100N65G2AG

Datasheet

Automotive-grade silicon carbide Power MOSFET 650 V, 20 mΩ typ., 100 A in an HiP247 package

HiP247

D(2, TAB)

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTW100N65G2AG	650 V	26 mΩ	100 A

- AEC-Q101 qualified
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitance
- Very high operating junction temperature capability (T_J = 200 °C)

Applications

- Main inverter (electric traction)
- DC/DC converter for EV/HEV
- On board charger (OBC)

Source: 6

Tesla Model 3 Inverter with STMicroelectronics
650V/100A SiC MOSFET


Source: 7

Tesla Model 3 - *2018*

Higher **blocking** voltages (>650 V) – Better **thermal** performance – Occupy **less space** compared to Si

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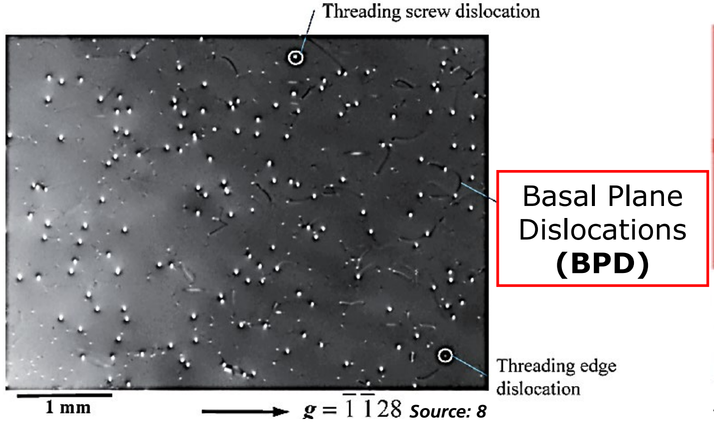
The challenges!

Bipolar Degradation (BD) in SiC PN devices

Background

Recombination induced stacking faults causing BD during operation



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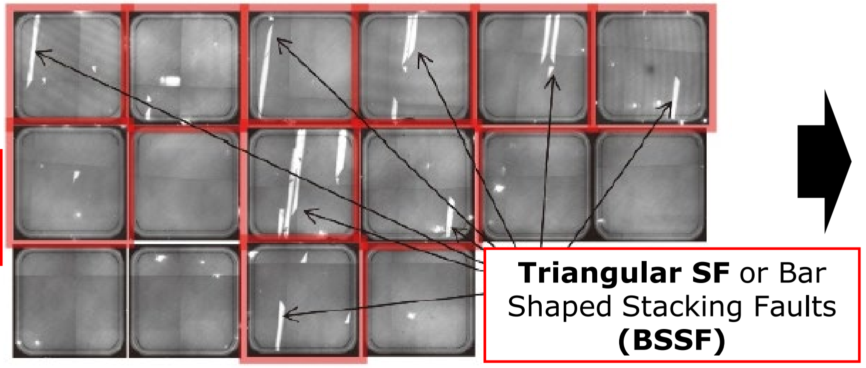

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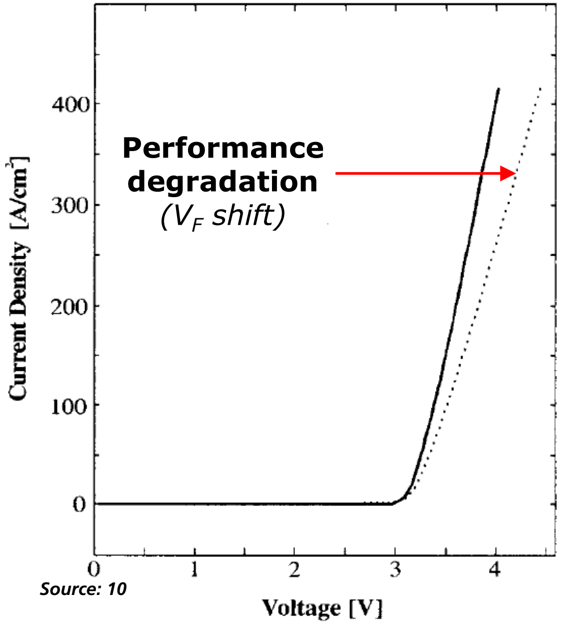

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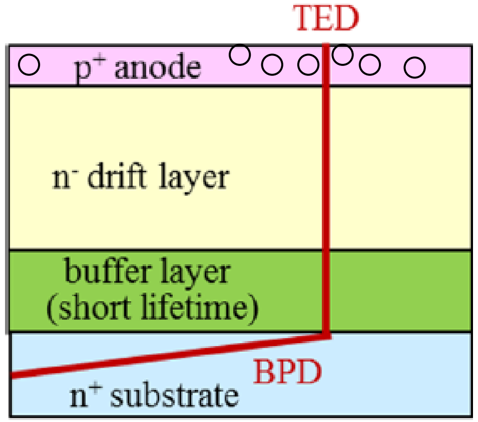

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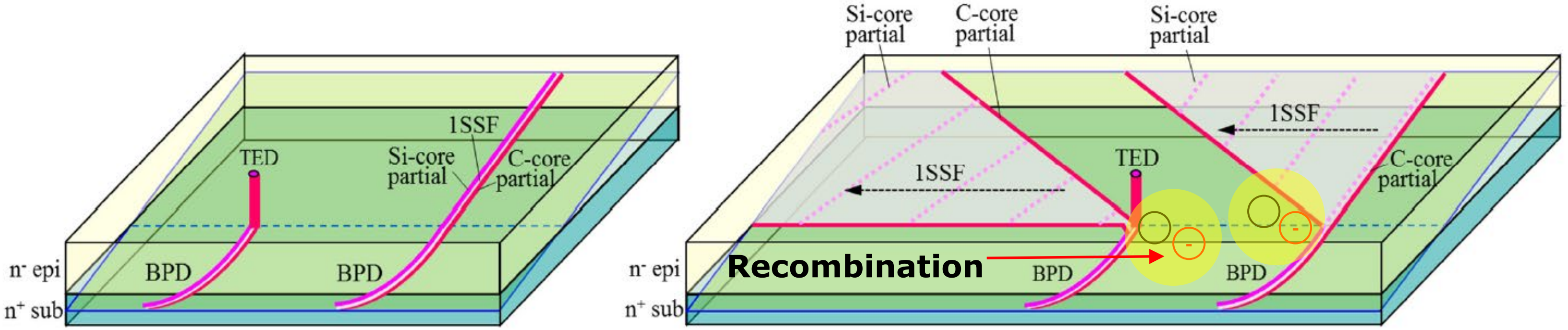


Propagation during processing

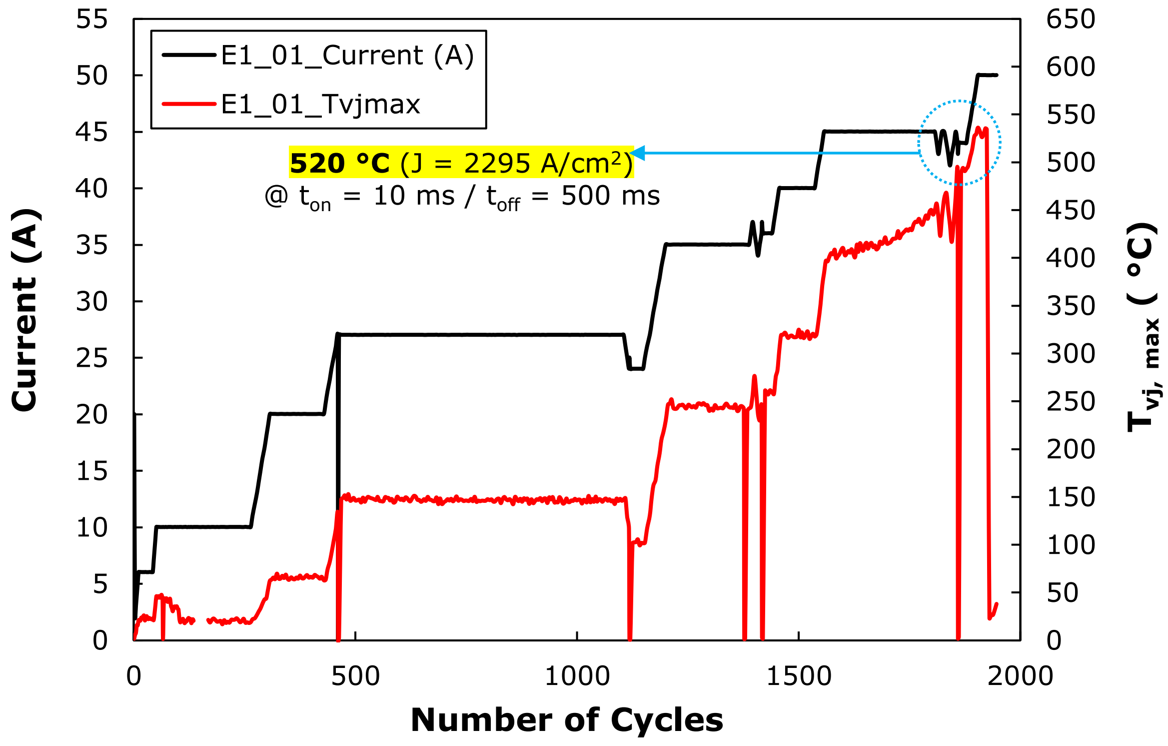
Expansion during device operation *(depends on current density)*

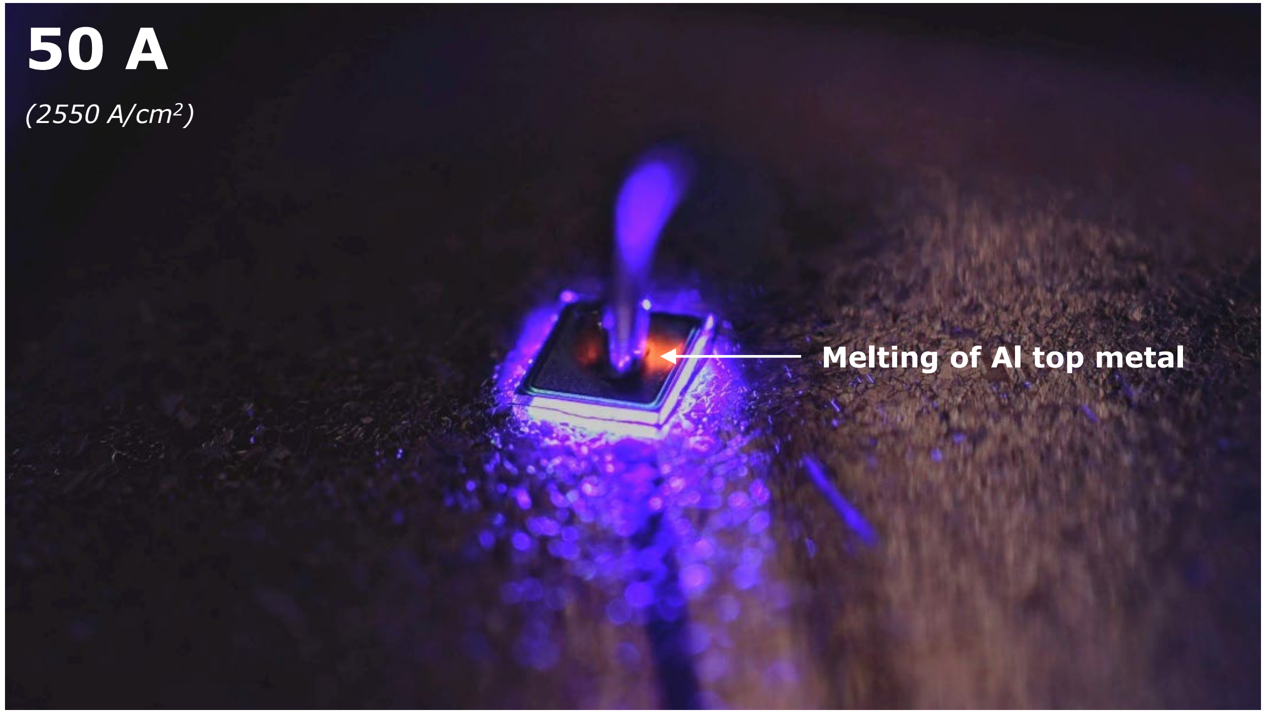
How to test Bipolar degradation in real world?

High current short pulse (10 ms)

Implementing high current density with controlled heating – *as per literatures*

Pulsed current for high current density and lower T_{vj}





Device temperature is close to Al melting temperature (660 °C)

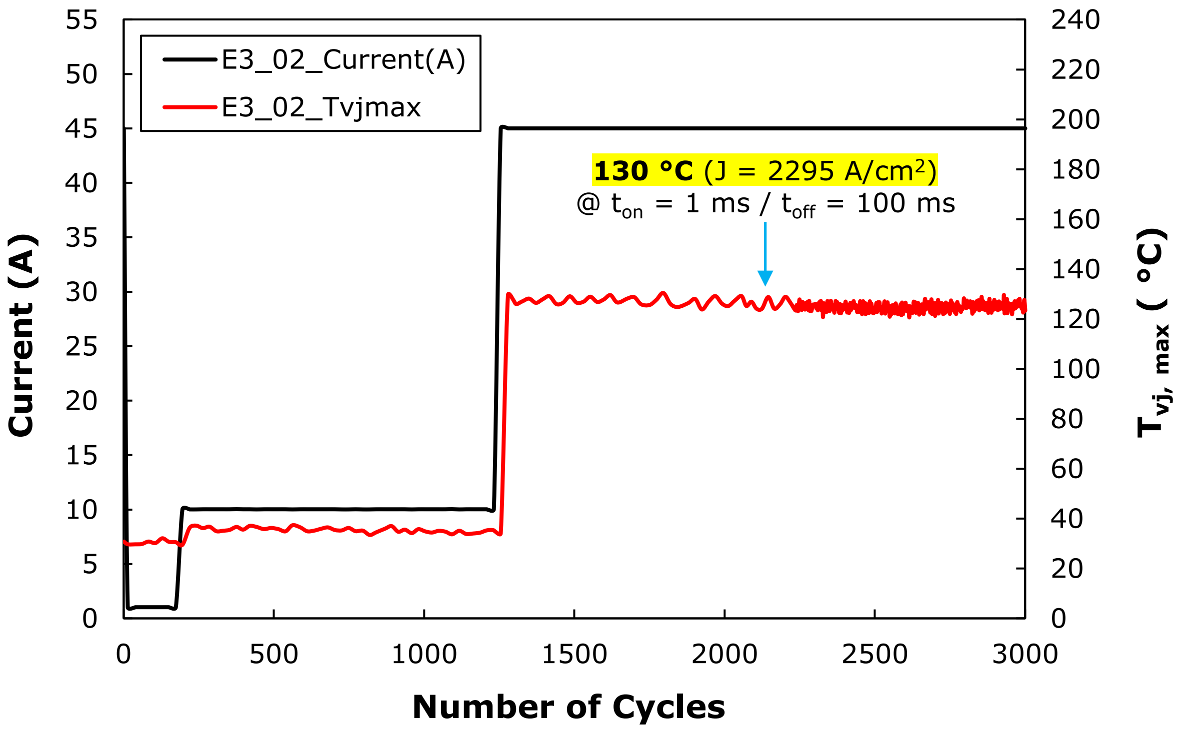
Device destruction in time

The solution?

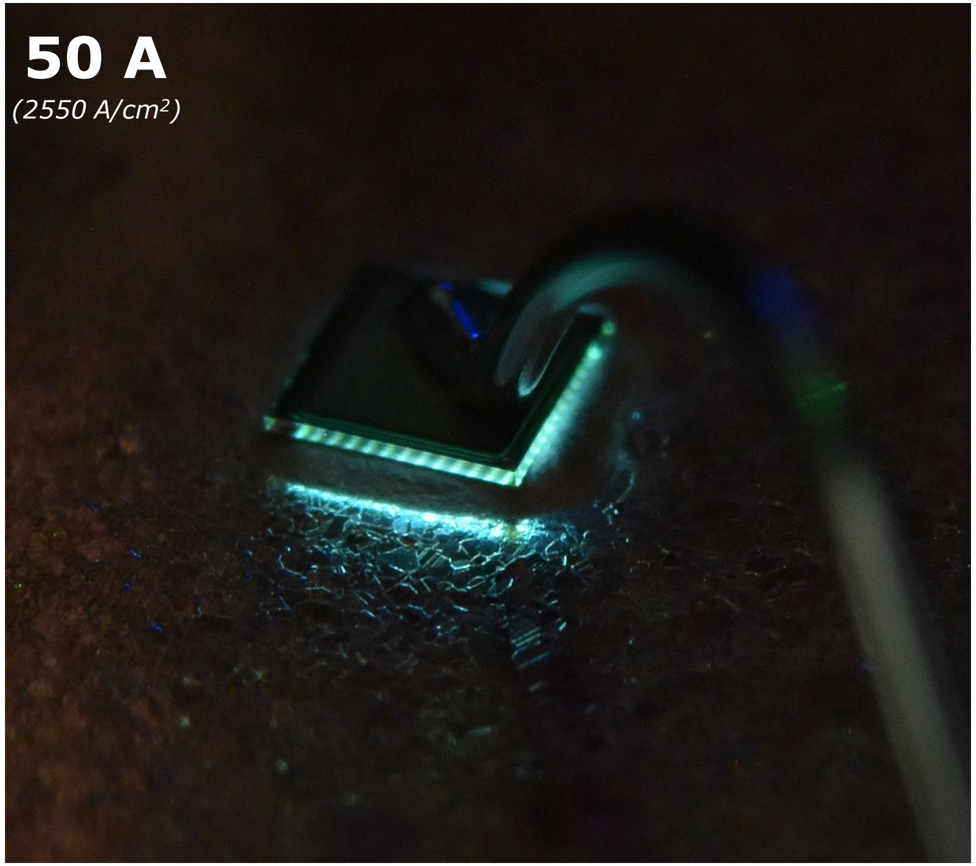
Power Cycling millisecond (PC_{msec} of 1 ms)

Replicating surge conditions while controlling device temperatures

High current density and control on $T_{vj,\,max}$



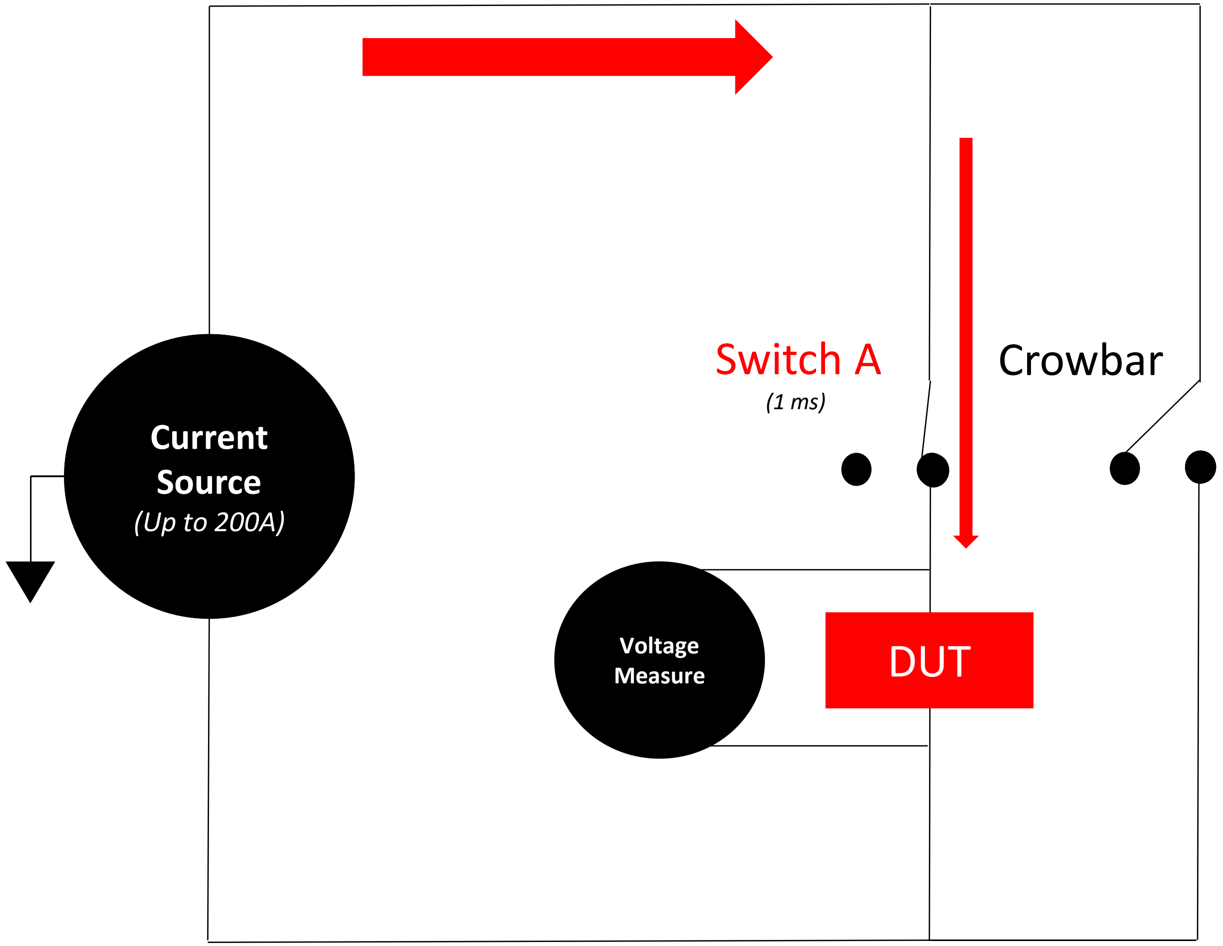
$T_{vj,\,max}$ is below maximum device temperature (175°C)
$T_{vj,\,max}$ is below chip solder melting point (240°C)



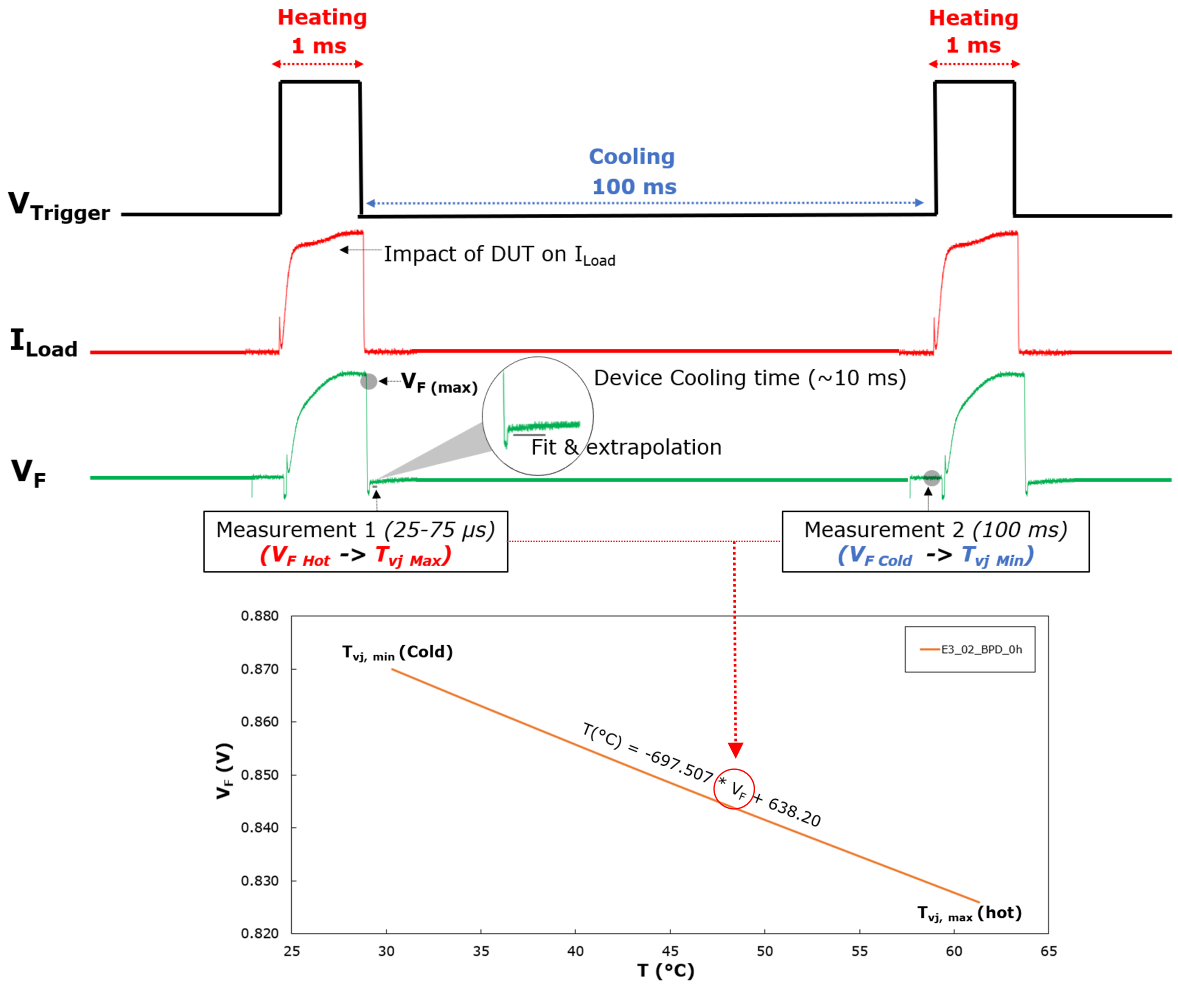
How to do this test?

Test Concept – Bipolar Degradation

Optimizing power cycling setup for short pulses



Test Schematic



Measurement Strategy

Device Technology Background

Conceptual description of the experimental DUTs

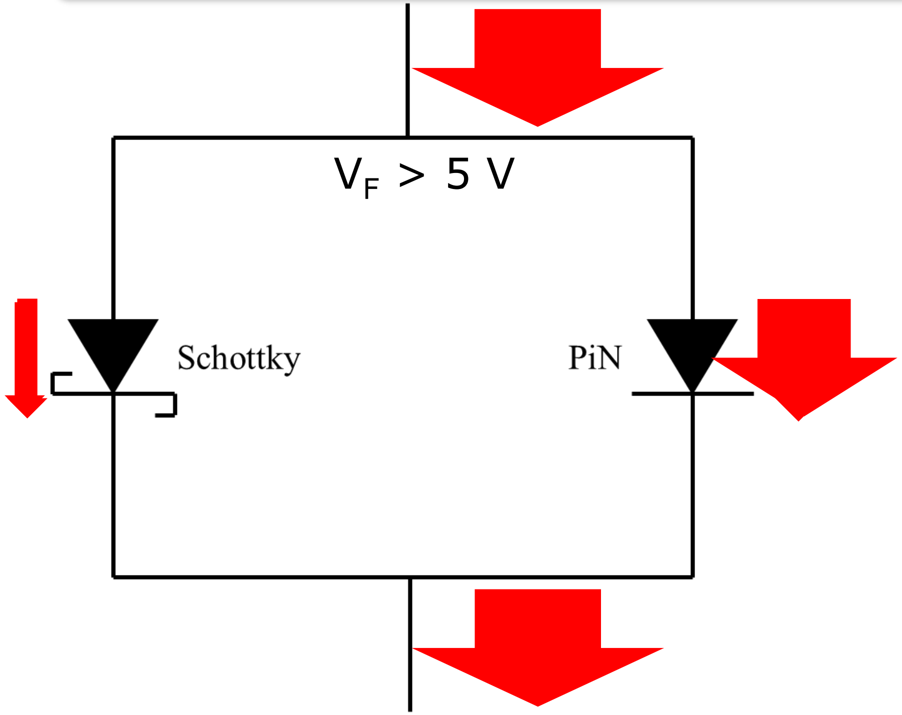
4H-SiC - Wide bandgap (Higher $\mathbf{V_{BR}}$)

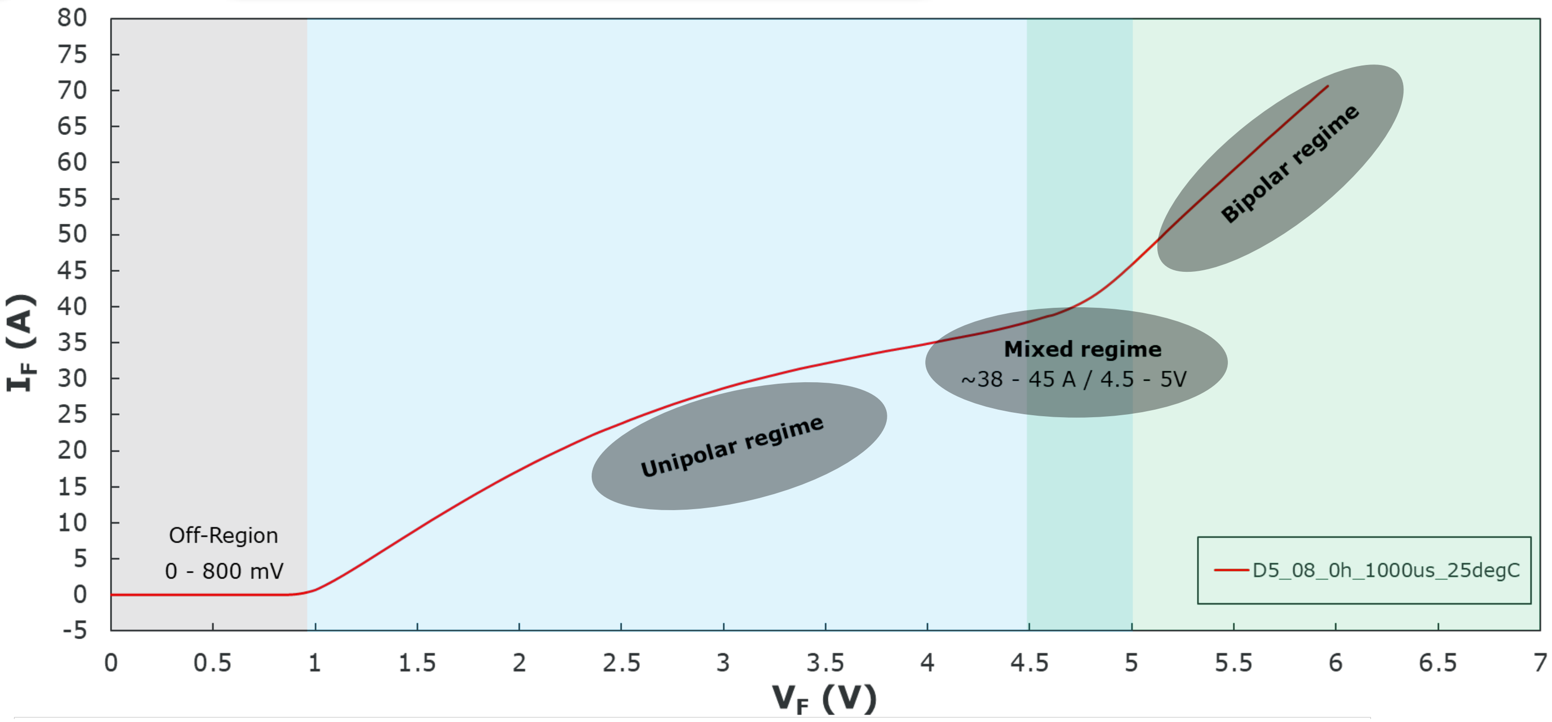
Schottky - Low $\mathbf{V_{th}}$

PiN - **Surge** current capability

Merged PiN Schottky (MPS)

(650 V / 10 A)





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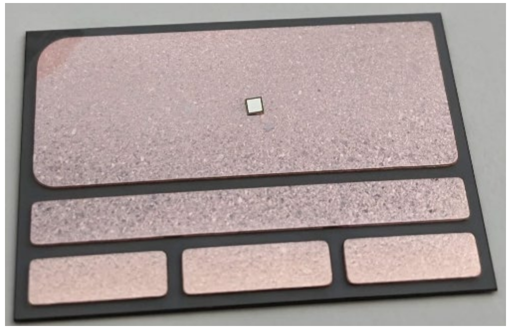
Things needed for experiment?

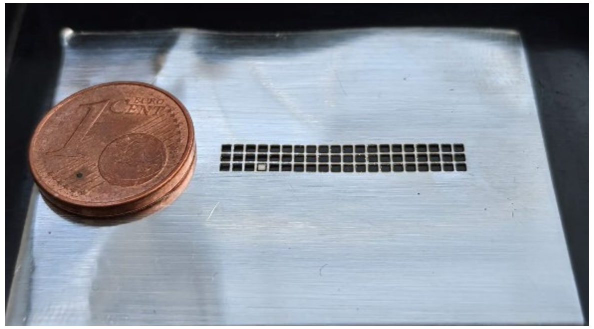
Sample Preparation - 1

Assembly of DUTs for test

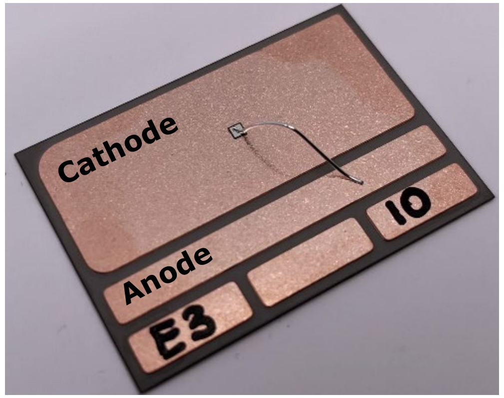
Bare die SiC MPS diode
(1.4 mm x 1.4 mm)



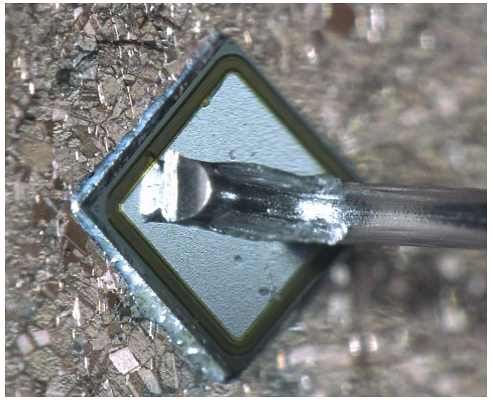
Chip placement on Si_3N_4 AMB substrate



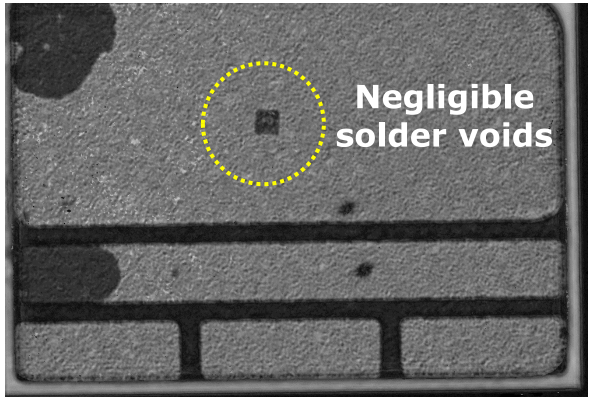
Laser cutting of Sn-Ag preforms
(800 µm x 800 µm)



Soldering and bonding for electrical connection



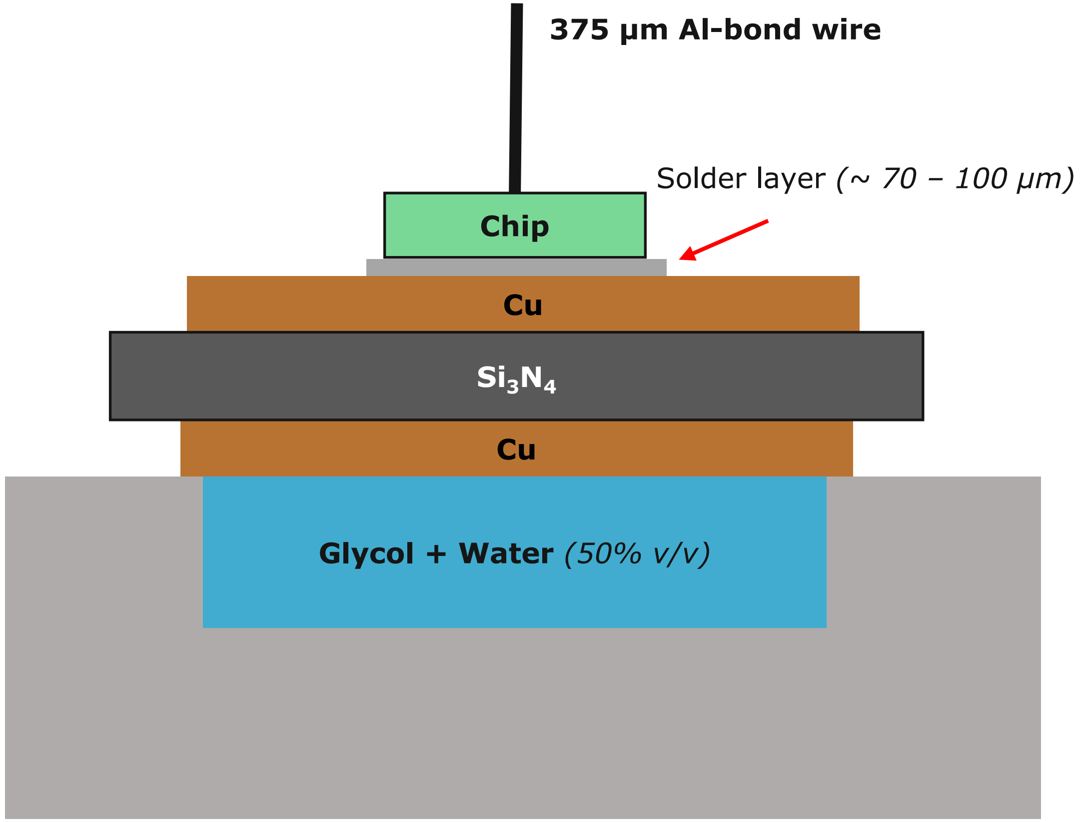
Visual inspection

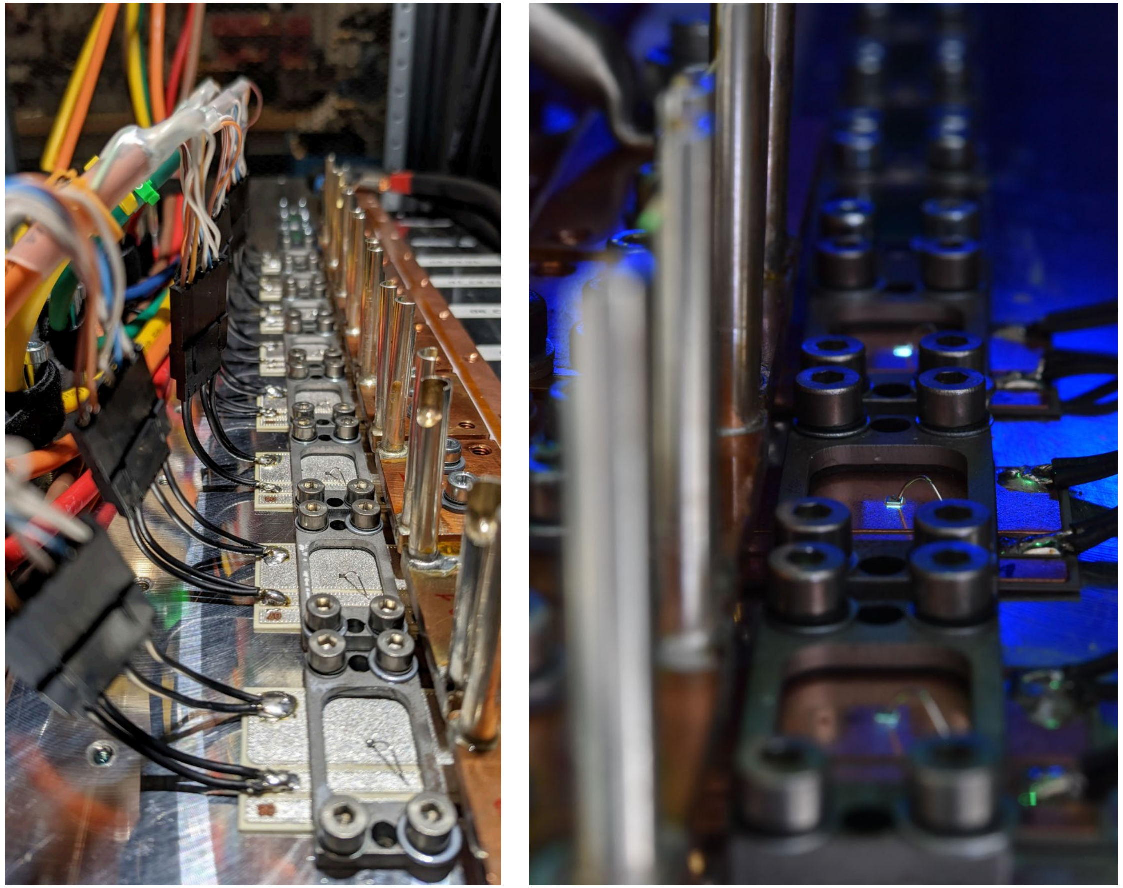


Inspection under Acoustic microscopy

DUT mounting

Assembly of bare dies in testbench





Bare dies mounted on testbench

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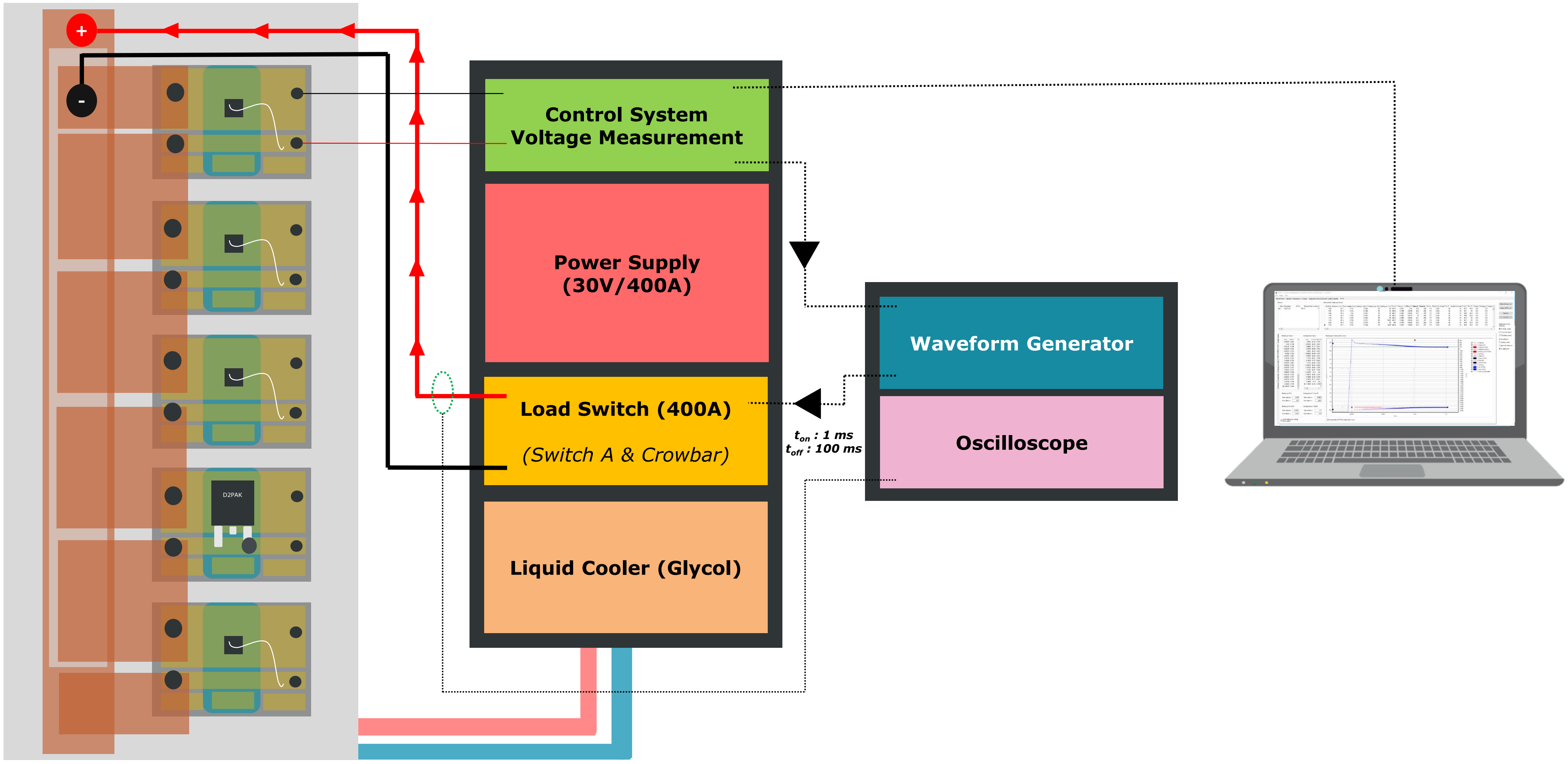
Experimental Setup – 1 (Schematic)

Setup overview



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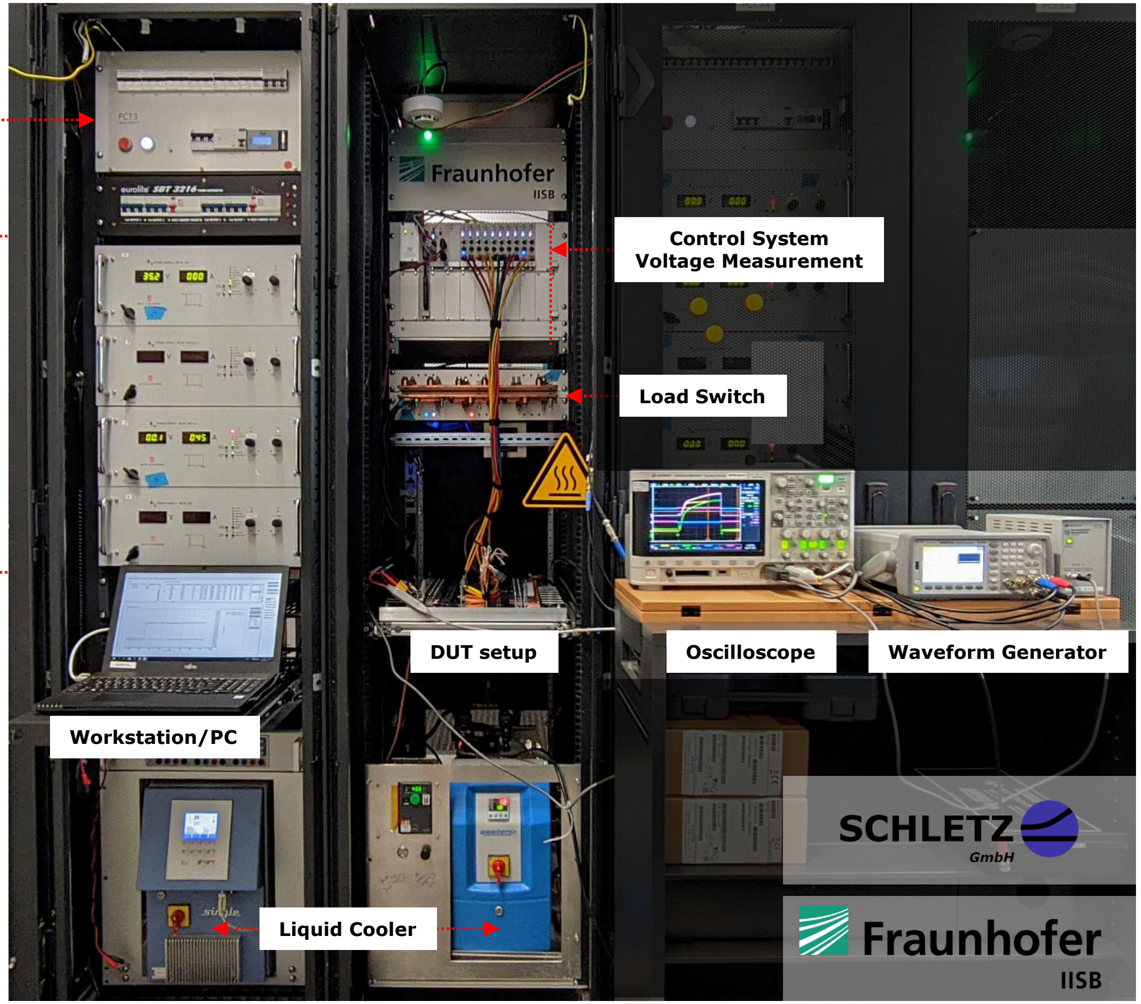
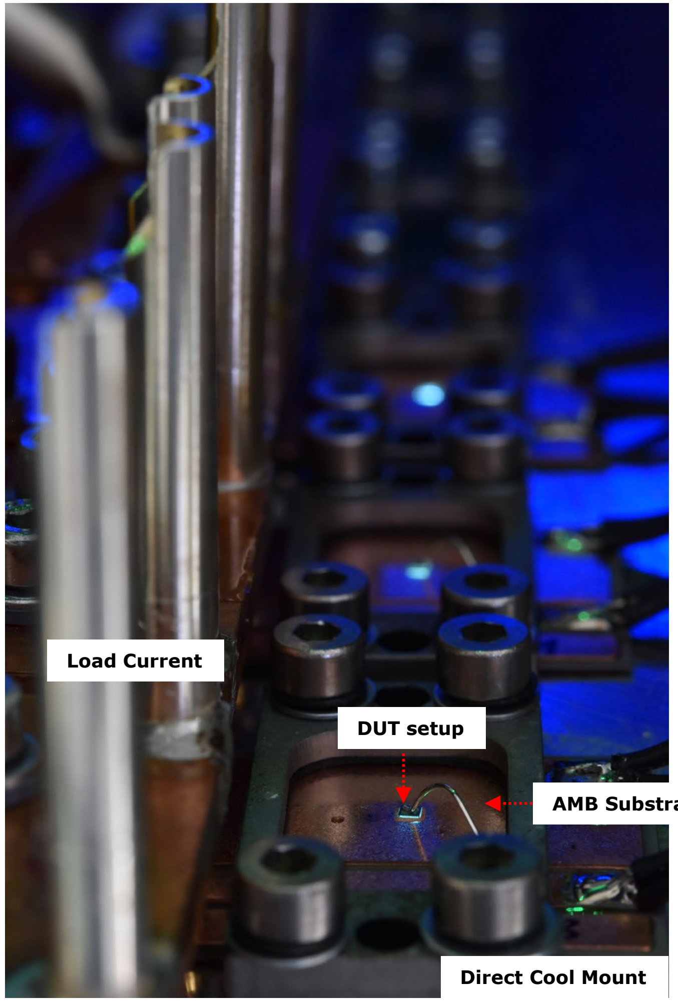
Experimental Setup – 2 (Implementation)

Description of the actual testbench





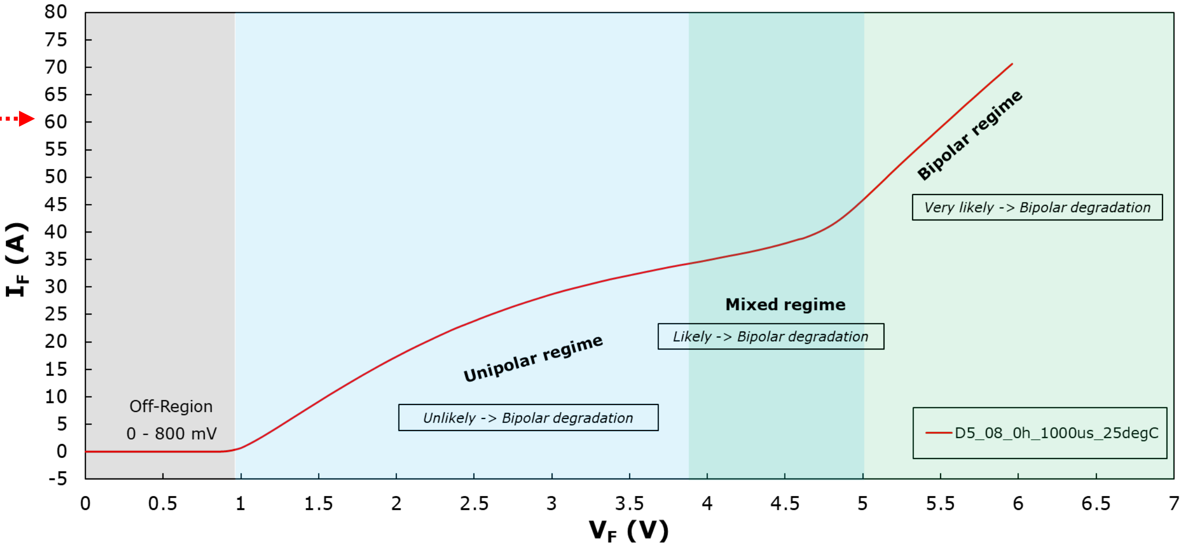
Running the test!

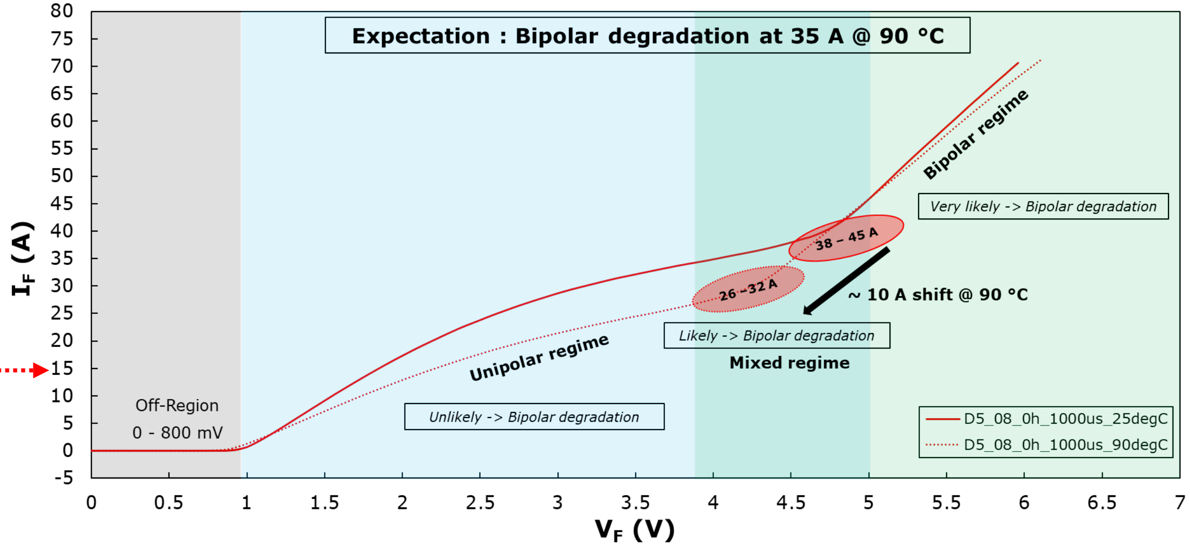
Test Strategy

Variation of current, temperature and die types

Pulsed heating current (1 ms)	T_a = 25 °C	T_a = 85 °C
35 A *(1785 A/cm²)* (Unipolar Regime)	✓ ✓ ✓ GD/BPD/SF	✓ ✓ GD/BPD/SF
45 A *(2295 A/cm²)* (Mixed Regime)	✓ ✓ ✓ GD/BPD/SF	✓ ✓ ✓ GD/BPD/SF
55 A *(2806 A/cm²)* (Bipolar Regime)	✓ ✓ ✓ GD/BPD/SF	✓ ✓ ✓ GD/BPD/SF

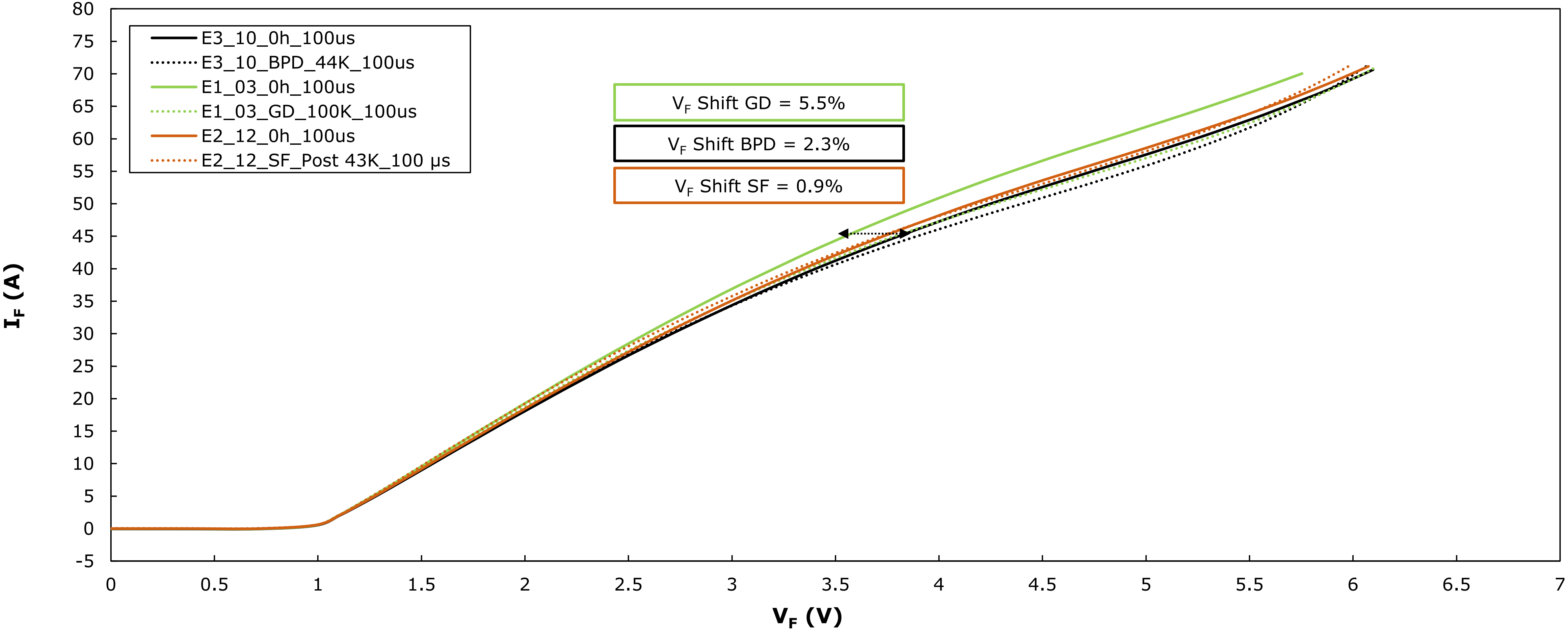
- *$T_{vj, max}$ is set to 240 °C to minimize solder degradation*





Pre/Post Characterization Results (45A) - 1

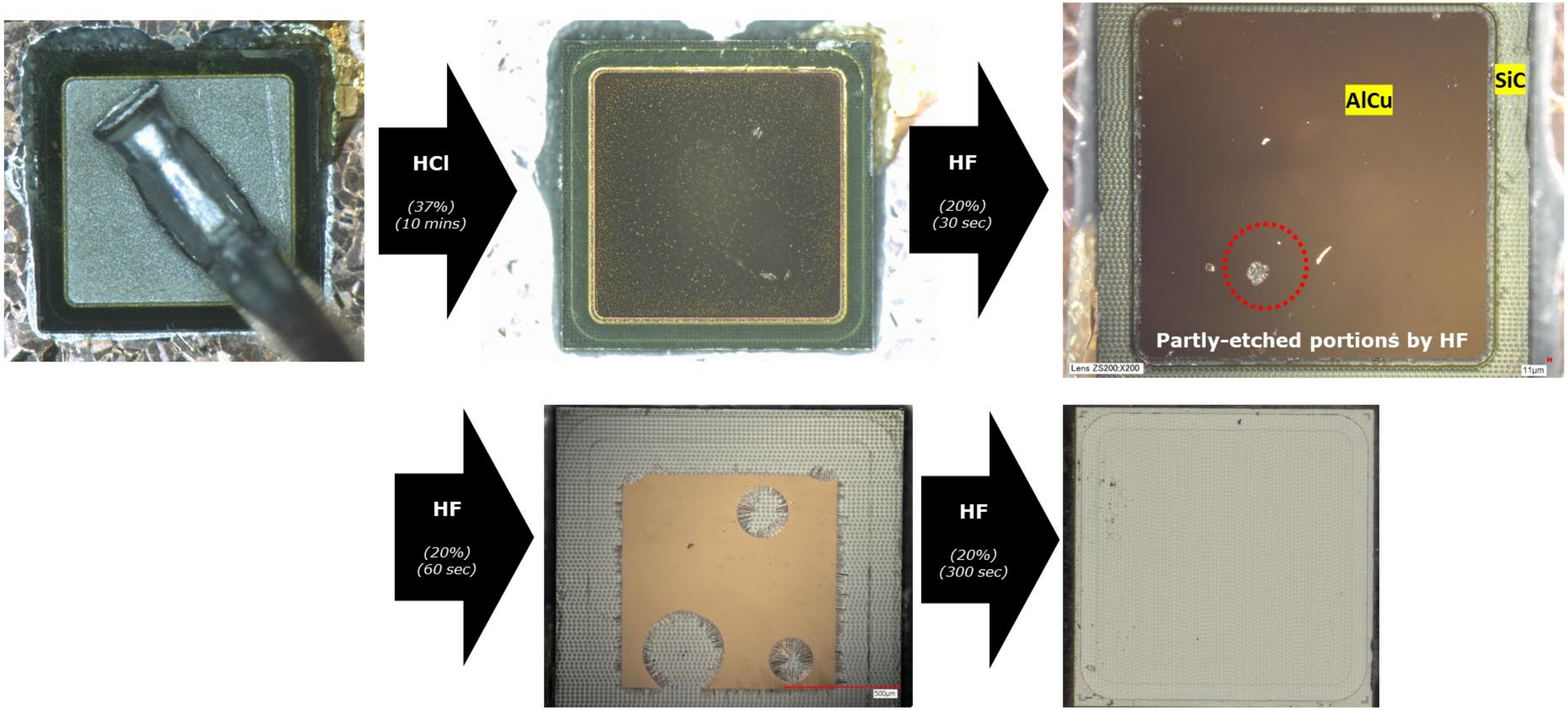
I-V Sweep measurement



- *Tested at room temperature : (T_a = 23 °C), Configuration : IF_{max} = 70 A, t_p = 100 µs*

Post-test failure analysis - 1

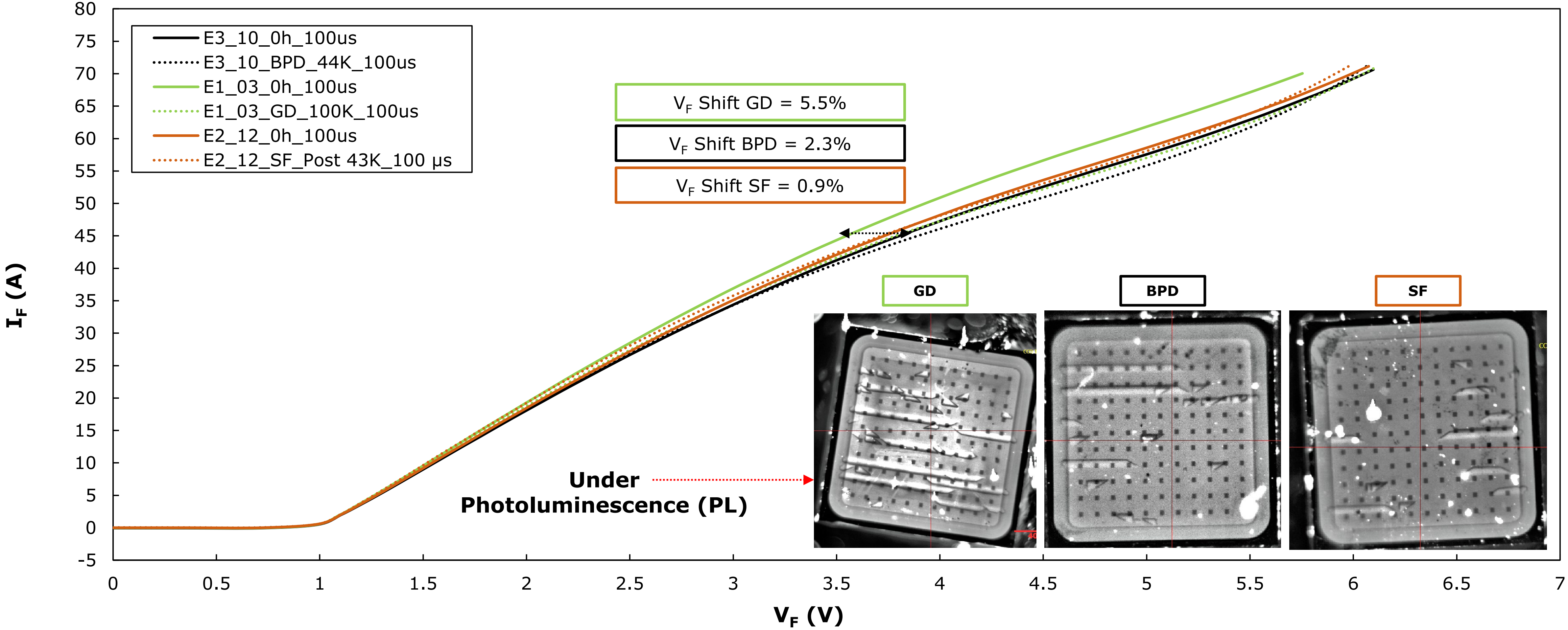
Removal of power and Schottky metal



- *The DUT was measured with VHX 7000 digital microscope with 100x magnification*

Pre/Post Characterization Results (45A) - 2

I-V Sweep measurement – Forward bias



- *Tested at room temperature : (T_a = 23 °C), Configuration : IF_{max} = 70 A, t_p = 100 µs*

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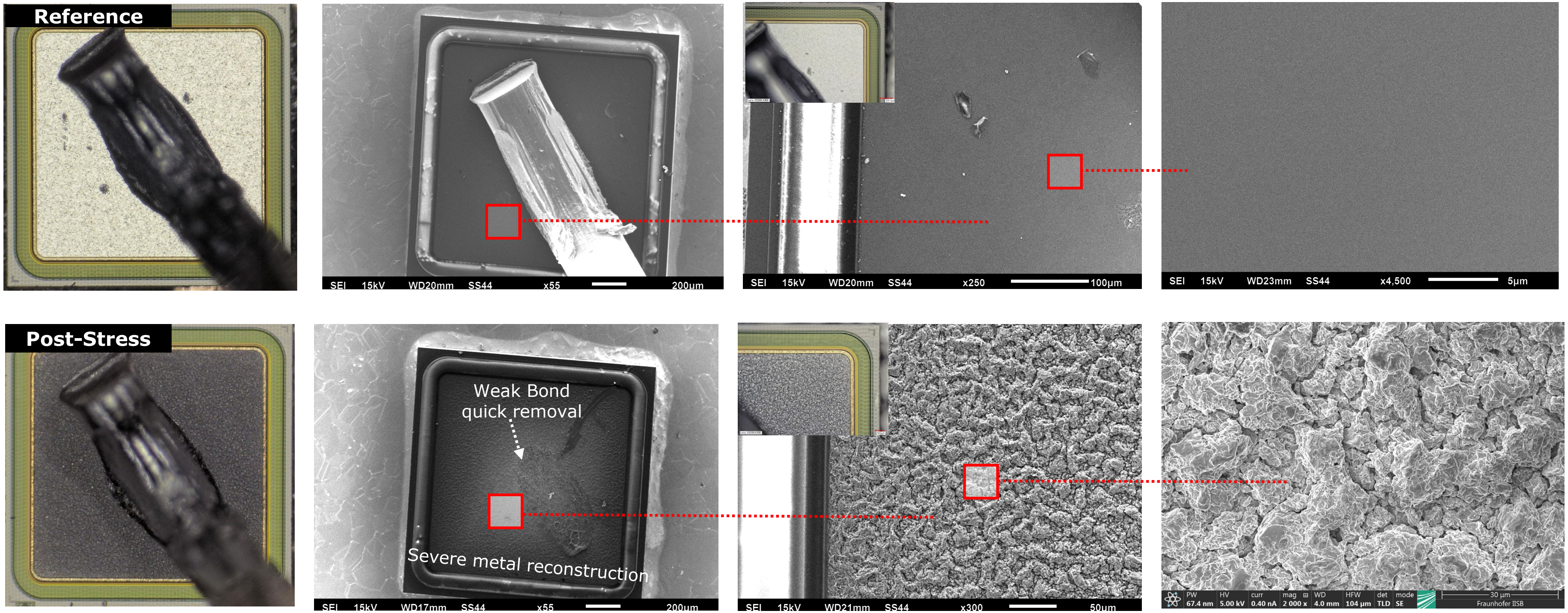
Post-test failure analysis - 2

Metal Reconstruction



- *The DUTs were inspected under JEOL-6610 Series Scanning Electron Microscope*

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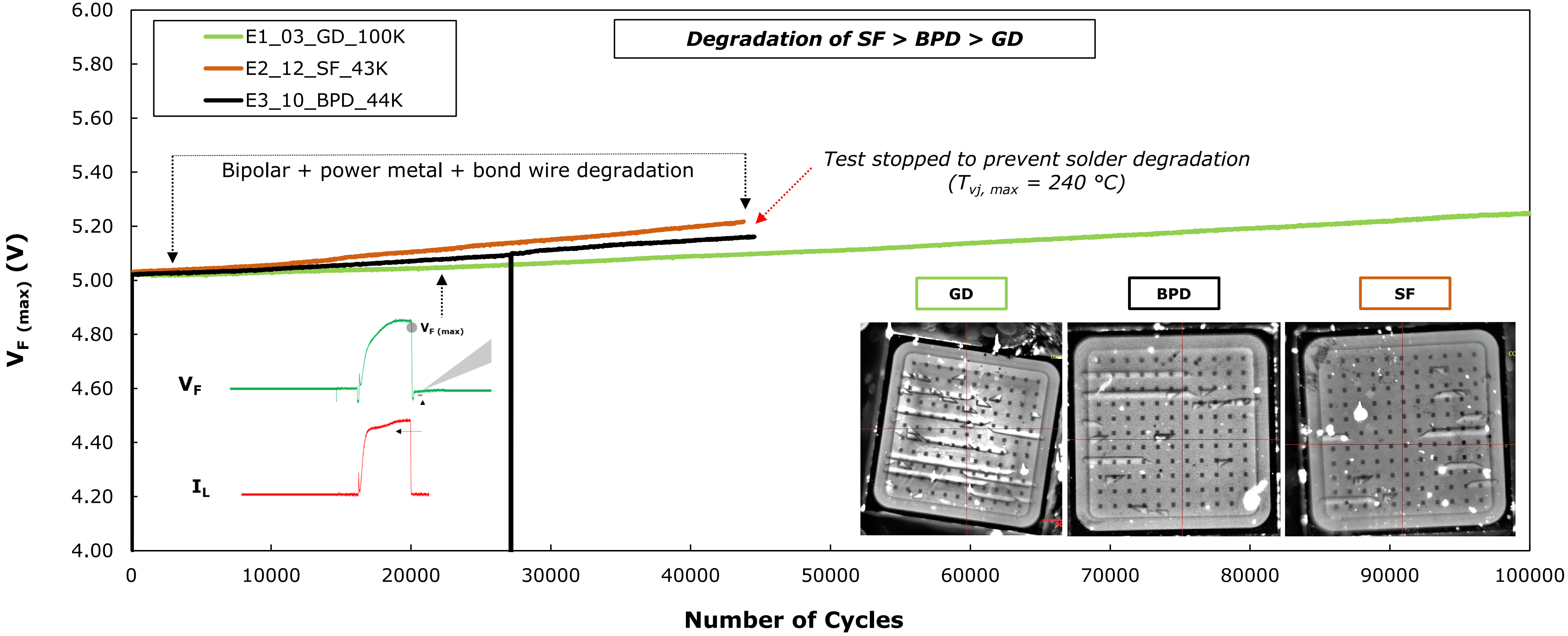
Variation of $V_{F\ (max)}$ over cycles

Heating V_F measurement during test



- *Test Parameters : Load Current = 45 A (Coolant Temperature = 25 °C (Glycol + water), t_{on} = 1 ms and t_{off} = 100 ms*

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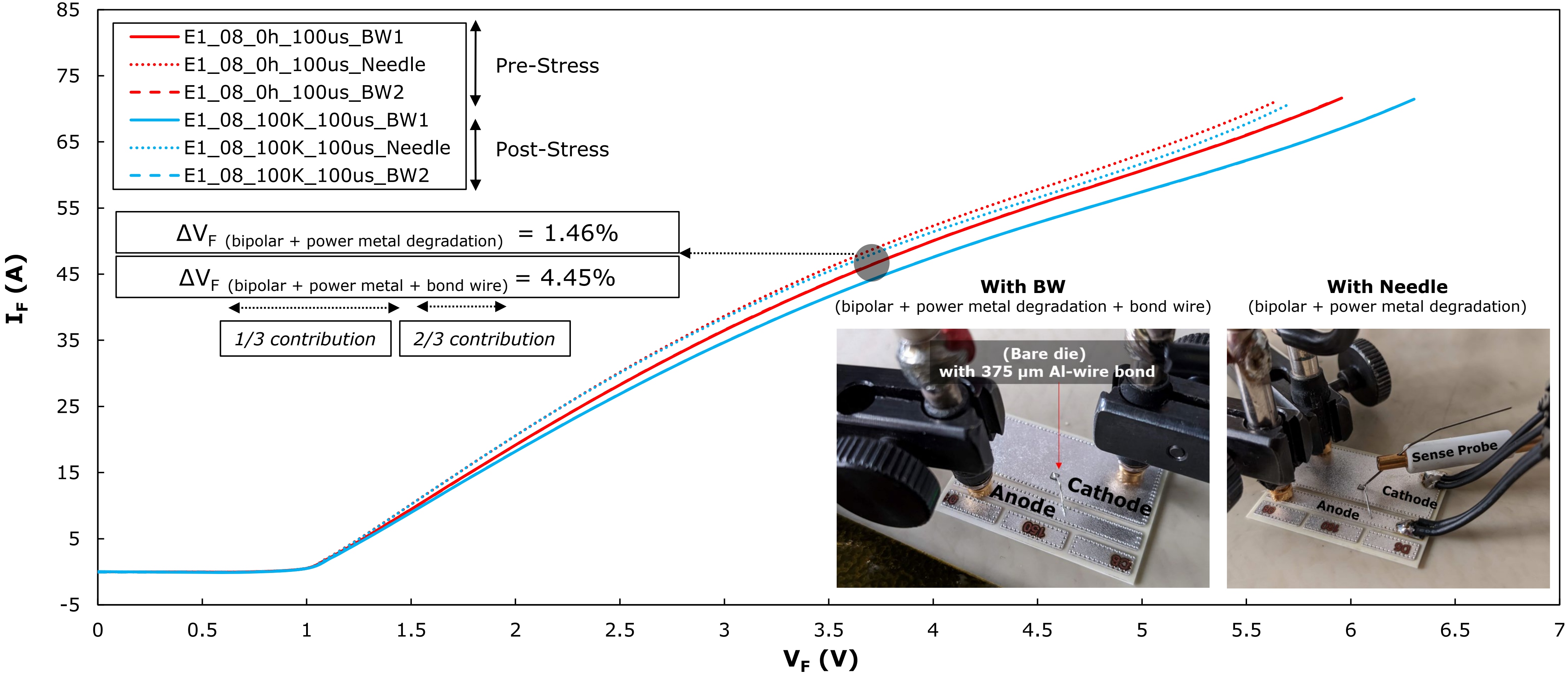
How much is the Bipolar vs. Thermal degradation?

Evaluating bipolar and thermal degradation

I-V Sweep with & w/o bond wire – Forward bias



- *Tested at room temperature : @ 22.1°C , Configuration : I_{max} = 70 A, t_p = 100 µs*

Summary

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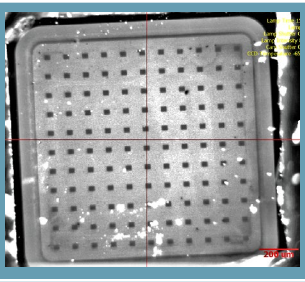
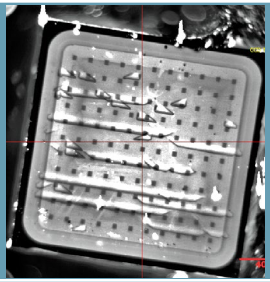
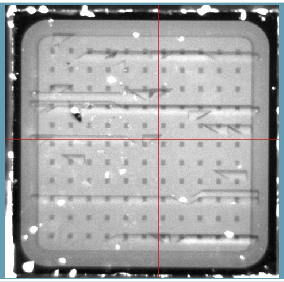
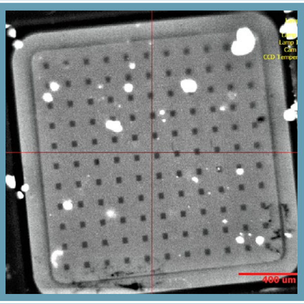
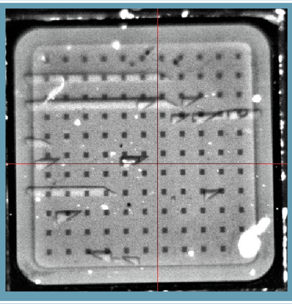
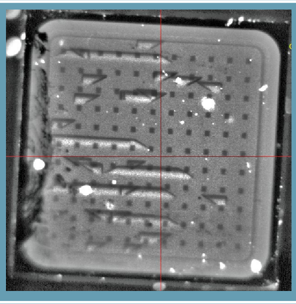
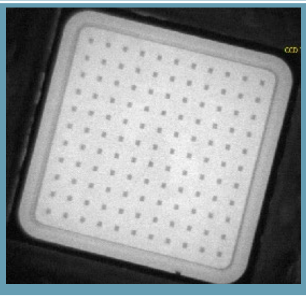
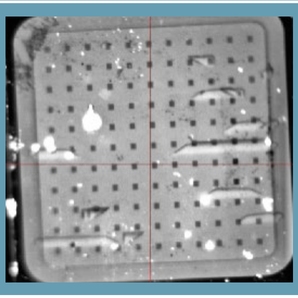
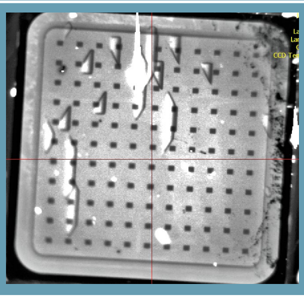
Overall Results after Photoluminescence

Tested samples after metal etch and PL scan

Current / Device Type	35A *(1785 A/cm²)*	45A *(2295 A/cm²)*	55A *(2806 A/cm²)*
GD	**E1_06**  **100 sec** *-4% shift*	**E1_03**  **100 sec** *5.5% shift*	**E1_04**  **32 sec** *13% shift*
BPD	**E3_15**  **100 sec** *0.5% shift*	**E3_10**  **44 sec** *2.3% shift*	**E3_11**  **13 sec** *7.3% shift*
SF	**E2_14**  **100 sec** *-3% shift*	**E2_12**  **43 sec** *0.9% shift*	**E2_11**  **6.5 sec** *6.7% shift*

Summary of results and findings

Highlights and lowlights based on test evaluation

	25 °C			85 °C		
	35A	45A	55A	35A	45A	55A
Bipolar degradation	✗	✓	✓	✗ (Does not depend on temperature)	✓	✓
Power metal degradation	✓	✓	✓	✓	✓	✓
Bond wire degradation	✓	✓	✓	✓	✓	✓
	Sample size : 38			Sample size : 9		

- *3 devices were test devices out of 50*

Inferences and future scope

Key pointers

Shorter t_p **<= 1 ms** is essential to **minimize thermal degradation**

BD occurred at **> 3.5 times $J_{nominal}$** or **>35 A**, regardless of temperature

Precise **Characterization without** relying on the **degraded** bond wire **interconnect**

Etching of the samples to **investigate** nucleation **source**

Measure **power metal degradation** using **four-point measurement** pre/post stress

Image References

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2. https://www.etsy.com/nz/listing/992754356/colorful-silicon-carbide-crystal
3. https://www.researchgate.net/publication/34444231_Lanthanide_doped_wide_band_gap_semiconductors_Elektronische_Ressource_intra-4f_luminescence_and_lattice_location_studies/figures?lo=1
4. https://www.powersystemsdesign.com/articles/how-sic-and-gan-enable-higher-power-conversion-efficiency/138/17281
5. https://www.pntpower.com/tag/device/
6. https://www.st.com/en/power-transistors/sctw100n65g2ag.html#documentation
7. https://www.pntpower.com/tesla-model-3-powered-by-st-microelectronics-sic-mosfets/

8. K. Omote, "Crystal defects in SiC wafers and a new X-ray topography system," in Proc. Conference Name, Year, pp. Page numbers. [Online]. Available: https://api.semanticscholar.org/CorpusID:30917668

9. H. Tsuchida, K. Murata, T. Tawara, M. Miyazato, T. Miyazawa and K. Maeda, "Suppression of Bipolar Degradation in 4H-SiC Power Devices by Carrier Lifetime Control," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 20.1.1-20.1.4, doi: 10.1109/IEDM19573.2019.8993530

10. P. Bergman, H. Lendenmann, P. Nilsson, U. Lindefelt, and P. Skytt, "Crystal Defects as Source of Anomalous Forward Voltage Increase of 4H-SiC Diodes," Materials Science Forum - MATER SCI FORUM, vol. 353-356, pp. 299-302, 2001. [Online]. Available: DOI: 10.4028/www.scientific.net/MSF.353-356.299.

Knowledge References

[1] P. Bergman, H. Lendenmann, P. Nilsson, U. Lindefelt, and P. Skytt, "Crystal Defects as Source of Anomalous Forward Voltage Increase of 4H-SiC Diodes," Materials Science Forum - MATER SCI FORUM, vol. 353-356, pp. 299-302, 2001. [Online]. Available: DOI: 10.4028/www.scientific.net/MSF.353-356.299.

[2] S. Palanisamy, T. Basler, J. Lutz, C. Künzel, L. Wehrhahn-Kilian, and R. Elpelt, "Investigation of the bipolar degradation of SiC MOSFET body diodes and the influence of current density," in 2021 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2021, pp. 1-6. [Online]. Available: DOI: 10.1109/IRPS46558.2021.9405183.10.1109/IRPS46558.2021.9405183.

[3] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, "Semiconductor Power Devices," 2018. [Online]. Available: DOI: 10.1007/978-3-319-70917-8, pp. 280.

[4] U. Scheuermann and R. Schmidt, "Impact of solder fatigue on module lifetime in power cycling tests," in Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 2011, pp. 1-10.

[5] Y. Ebihara et al., "Suppression of Bipolar Degradation in Deep-P Encapsulated 4H-SiC Trench MOSFETs up to Ultra-High Current Density," in 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2019, pp. 35–38.

[6] K. Omote, "Crystal defects in SiC wafers and a new X-ray topography system," in Proc. Conference Name, Year, pp. Page numbers. [Online]. Available: https://api.semanticscholar.org/CorpusID:30917668

[7] S. Palanisamy, J. Kowalsky, J. Lutz, T. Basler, R. Rupp, and J. Moazzami-Fallah, "Repetitive surge current test of SiC MPS diode with load in bipolar regime," in 2018 IEEE 30th International Symposium

Thank You for your attention

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