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SiC VDMOS Technology with Self-Aligned Channel

Processed 150 mm 4H-SiC wafer with 1.2 kV VDMOS transistors

Silicon carbide (SiC) power MOSFETs combine the features of nearly ideal switching with superior electrical and thermal properties of wide-bandgap semiconductor materials. High breakdown voltage of the vertical device is supported on a high-quality epitaxial layer, while threshold voltage and electrical current transport are precisely defined by ion implantation. Top and bottom sides of the devices are metallized for assembly in power modules.

The on-state resistance for power MOSFETs is still dominated by the channel resistance, especially for voltage classes below 3 kV. Therefore, an optimized channel design is of high importance for a high-performance device. Technological limitations, like overlay accuracy of the lithography, can lead to a reduction of blocking voltage due to short channel effects for edge-of-technology channel design. To reduce the influence of technological parameters for high yield at small channel length, a self-aligned channel process has been introduced.

After the first implantations, a thick polysilicon layer is deposited on the scattering oxide. The hard mask is structured by dry etching, with etch stop on the oxide. This hard mask serves as an ion-stop for the PWELL aluminum implantation. Subsequently, a nitride layer is deposited. The layer thickness of this layer defines the channel length. By anisotropic dry etching of this layer, a spacer is formed. The NPLUS (source) implantation is performed with the now modified hard mask.

Advantages

- Typical $R_{DS(on)}$ below 7 mΩ·cm² for 1.2 kV
- Homogeneous channel length over the wafer
- Independent of lithography misalignment
- Channel length can be controlled by processing parameters (nitride film thickness)
- High temperature implantation with self-aligned channel hard mask

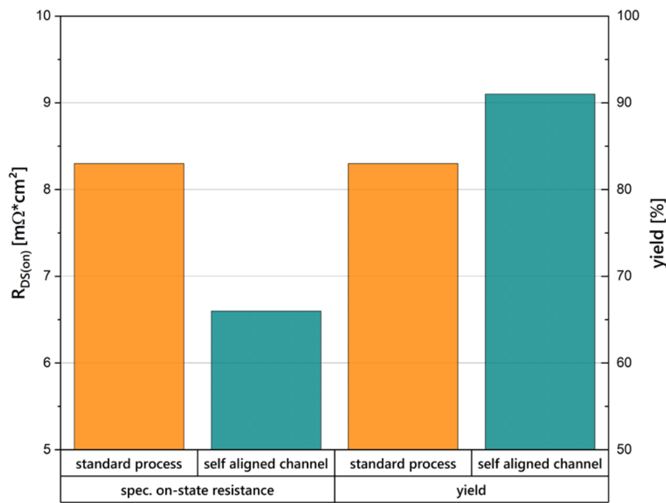

Fig. 1: On-state resistance ($R_{DS(on)}$) and yield values for power MOSFET devices processed with standard lithography process (channel 1 µm) and self-aligned channel process (channel 0.6 µm)

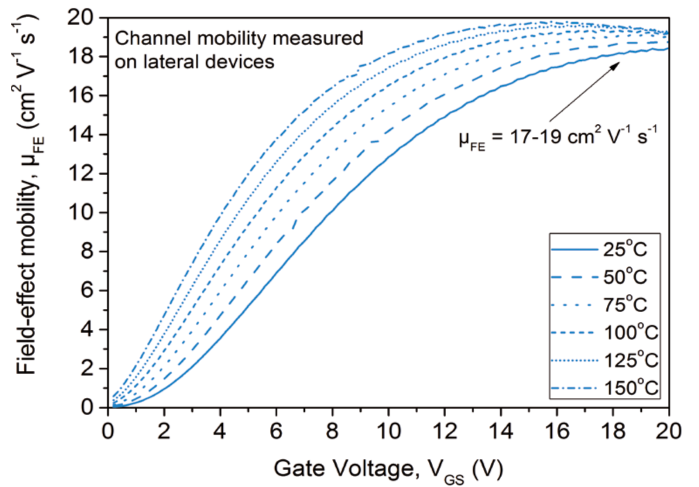

Fig. 4: Example of process technology optimization: Oxide and semiconductor / oxide interface optimized for channel mobility and lifetime

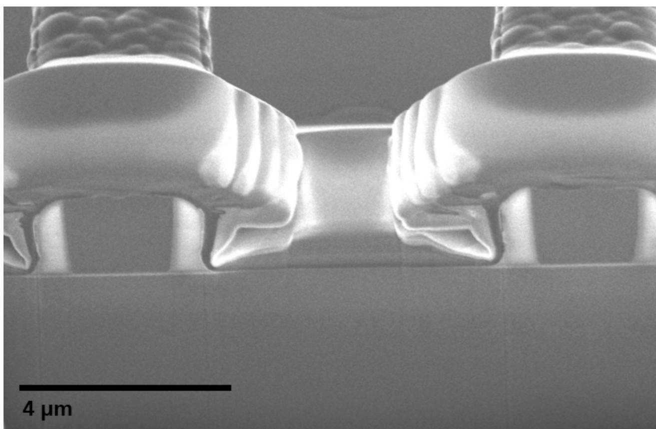

Fig. 2: FIB-cross section of self-aligned channel hard mask after structuring of nitride spacer

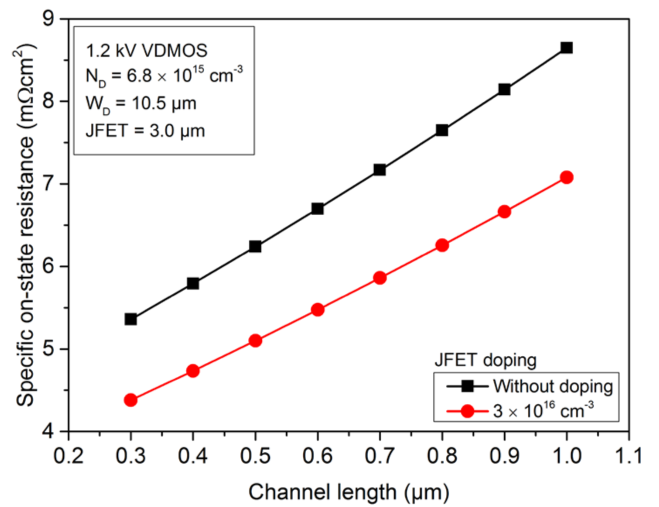

Fig. 5: Specific on-state resistance in dependence of channel length for power MOSFET with and without JFET implantation

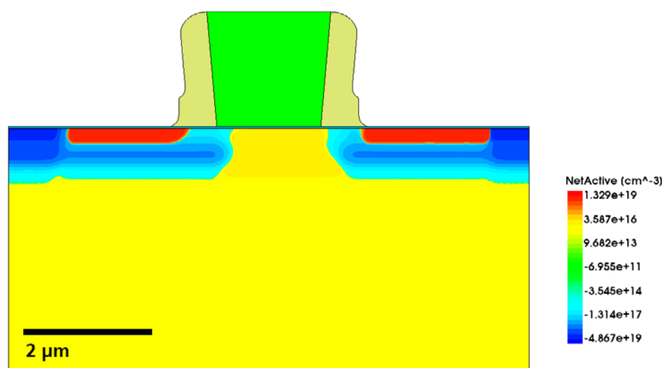

Fig. 3: Process simulation results for self-aligned channel process (hard mask structuring)

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