

Monolithically Integrated SiC Circuit Breaker

Self-Supplied, Self-Sensed and Self-Sustained up to 900 V_{DC}

150mm »SiC DC-Breaker« wafer fabricated at Fraunhofer IISB

For high power DC applications, the development of solid state circuit breakers (SSCB) is necessary and has seen a variety of different approaches. The proposed prototypes represent the first monolithically integrated 900 V SSCBs realised in a scalable 4H-SiC JFET technology. With this novel concept, the effort of interrupting excessive DC current in case of failure is reduced from a whole system (e.g. sensor, μC , power switch, gate driver) to a single two pole device. Furthermore, the proposed plug-and-play SSCB stands out through ultra fast response time, while showing excellent avalanche capability. The scope of future developments focuses on scaling the trigger current level to several 10 A per chip to address the requirements of power electronic applications in DC grid and e-mobility environments.

»Thyristor Dual« Topology (Fig. 1a)

- Two complementary normally-on JFETs
- V_{DS} of one JFET is equal to V_{GS} of other JFET
- Intrinsic current controlled blocking mechanism

Monolithic Integration (Fig. 1b)

- 4H-SiC JFET technology revolves around re-epitaxy and SiC dry etching
- pJFET buried in the 1st epitaxial layer
- nJFET located in the 2nd epitaxial layer
- Floating source terminal (S) allows for observation of operating conditions

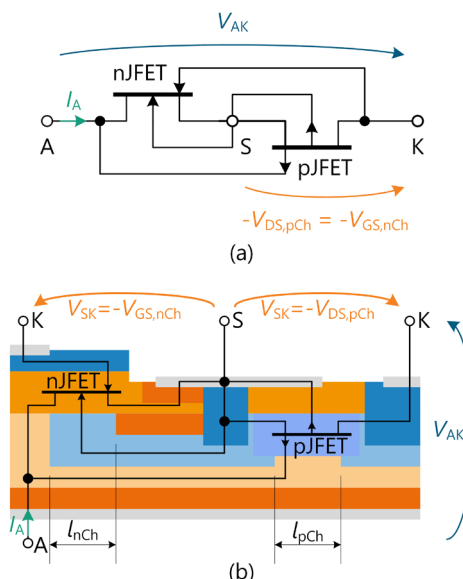


Fig. 1: Equivalent circuit diagram (a) and schematic cross section of the proposed monolithically integrated circuit breaker (b) [1, 2]

[1] N. Boettcher and T. Erlbacher, "A Monolithically Integrated SiC Circuit Breaker," IEEE Electron Device Letters, 2021.

[2] N. Boettcher and T. Erlbacher, "Fabrication Aspects and Switching Performance of a [...] Circuit Breaker Device," ISPSD, 2022.

Analytical and Numerical Modelling (Fig. 2)

- Technology is extensively described in simulation models
- TCAD models allow for predictive cell design

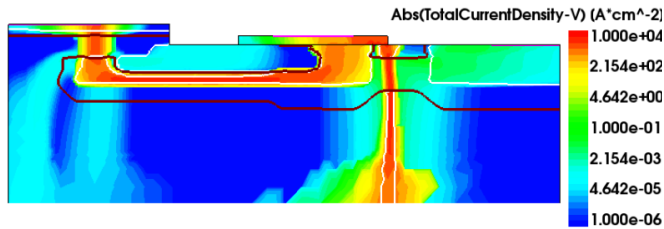


Fig. 2: TCAD simulation showing current flow under breakdown condition (reach-through) [3]

Scalable Output Characteristics (Fig. 3)

- Low resistive linear on-state region
 $R_{on,sp} \geq 650 \text{ m}\Omega\text{cm}^2$
- Self-sensed trigger mechanism
 $J_{trig} \leq 2.2 \text{ Acm}^{-2}$
- Self-sustained blocking state
 $V_{rt} \leq 900 \text{ V}$

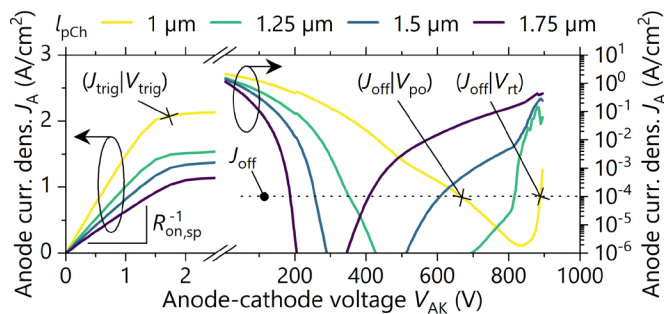
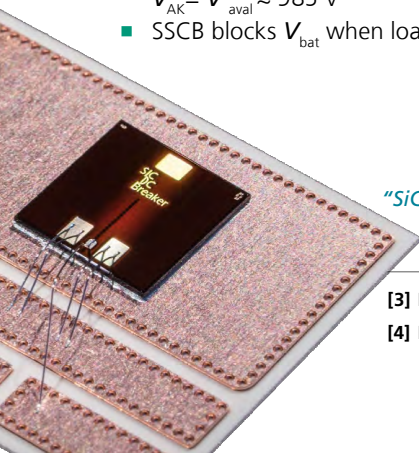


Fig. 3: Measured quasi-static output characteristics $J_A(V_{AK})$ for specific pJFET channel length values l_{pCh} [2]

Excellent Avalanche Capability during UIS (Fig. 4)

- Unclamped inductive switching (UIS) behaviour comparable to state-of-the-art power switches
- Intrinsic blocking mechanism triggered at
 $I_A = I_{trig} = 1.75 \text{ A}$
- SSCB conducts load current in avalanche state at
 $V_{AK} = V_{aval} \approx 985 \text{ V}$
- SSCB blocks V_{bat} when load current has fully subsided



“SiC DC-Breaker” chip on Cu substrate

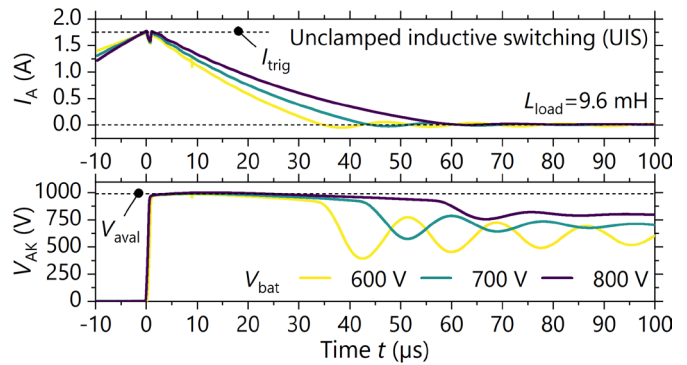


Fig. 4: Measured UIS response of anode current I_A and anode-cathode voltage V_{AK} for specific battery voltage values V_{bat} [2]

Ultra Fast Short Circuit Clearance (Fig. 5)

- Hard short circuit applied over the inductive load L_{load} at
 $I_A = 1 \text{ A}$ and $V_{bat} = 800 \text{ V}$
- SSCB blocks V_{bat} within $\sim 100 \text{ ns}$
- 5-10 times faster than state-of-the-art SSCBs

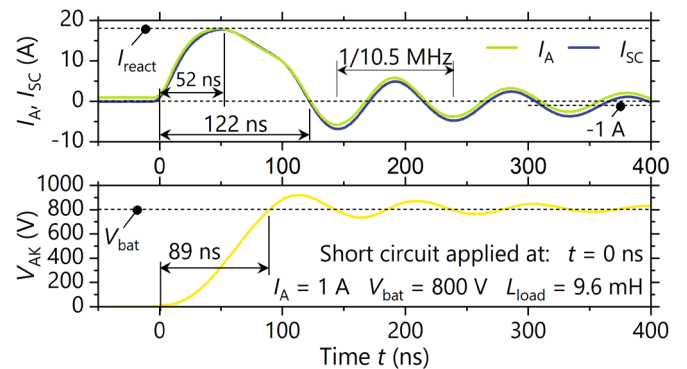


Fig. 5: Measured short circuit response of anode current I_A , short circuit current I_{SC} and anode-cathode voltage V_{AK} [4]

Contact

Norman Böttcher
 Semiconductor Devices
 Tel. +49 9131 761-605
 norman.boettcher@iisb.fraunhofer.de

Fraunhofer IISB
 Schottkystrasse 10
 91058 Erlangen, Germany
 www.iisb.fraunhofer.de



[3] N. Boettcher and T. Erlbacher, “Design Considerations on a [...] 900 V SiC Circuit Breaker,” WIPDA Asia, 2020.

[4] N. Boettcher et al., “Short Circuit Performance and Current Limiting Mode of a [...] SiC Circuit Breaker [...],” EPE, 2022.