Fraunhofer
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Fraunhofer Institute for Integrated Systems and Device Technology IISB

Early access to IISB's high temperature 4H-SiC CMOS (HT CMOS) technology

IISB @ EUROPRACTICE

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EUROPRACTICE

IISB's HT CMOS technology enables fabrication of integrated analog & digital circuits on 150 mm wafers which can operate at temperatures up to approx. 600 °C.

Custom solutions also allow for integration of sensors, e.g. UV and temperature, as well as lateral power devices. To support circuit design, a preliminary process design kit (PDK) based on KLayout and Cadence including technology information, process constrains, such as design, and layout rule checks (DRC & LVS) is provided.

EUROPRACTICE offers multi project wafer (MPW) technology runs, giving customers the opportunity to pay only for a selected design area. This reduces the entry barrier regarding costs and quantity, allowing academia and SMEs access to advanced technologies.

www.iisb.fraunhofer.de/europractice